Q.P. Code: 19EC0401 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Regular Examinations July-2021

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Convert the following numbers to Decimal and then to Octal. **i)** $(423416)_{10}$. **ii)** $(10010011)_2$.	L1	**6M**
	b	Convert the following to Decimal and then to Hexadecimal. **i)** $(1234)_8$ **ii)** $(11001111)_2$	L1	**6M**

OR

2	**a**	Simplify the following Boolean functions to minimum number of literals **i)** xyz + x'y + xyz'. **ii)** xz + x'yz.	L3	**6M**
	b	Simplify the following Boolean functions to minimum number of literals: F = ABC + ABC' + A'B	L3	**6M**

UNIT-II

3		Simplify the following Boolean expressions using K-map. F(A, B, C, D)= Σm(5,6,7,12,13)+ Σd(4,9,14,15)	L3	**12 M**

OR

4		What are the universal gates? Implement logic gates by using NAND and NOR gates.	L2	**12 M**

UNIT-III

5		Design 32:1 MUX using two 16:1 MUX'S and one 2:1 MUX.	L5	**12 M**

OR

6		What is magnitude comparator? Design 2-bit comparator by using logic gates.	L1	**12 M**

UNIT-IV

7		What is Register? Explain **i)** Parallel in Parallel out Register. **ii)** Series in Parallel out Register.	L3	**12 M**

OR

8	**a**	Explain working of Master Slave Flip flop with neat diagram.	L1	**6M**
	b	Draw the logic diagram T Flip Flop by using JK Flip Flop and draw the timing diagram.	L1	**6M**

UNIT-V

9		Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7).	L3	**12 M**

OR

10		Explain the following related to sequential circuits. **i)** State diagram. **ii)** State table. **iii)** State assignment.	L2	**12 M**

*** END ***